SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY
Accredited by National Board of Accreditation, AICTE, New Delhi, Accredited by NAAC with "A" Grade – 3.32 CGPA
Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi.
Permanent Affiliation to JNTUK, Kakinada
SEETHARAMPURAM, W.G.DT., NARSAPUR-534280, (Andhra Pradesh)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TEACHING PLAN

Course Code	Course9 Title	Semester	Branch	Contact Period /Week	Academic Year	Semester Commencement Date
20EC3T02	Digital Electronics (R-20)	III	ECE	5	2021-22	25-10-2021

COURSE OUTCOMES

After completion of the course student are able to

1	Describe the different types of number systems and Boolean algebra.(K1)
2	Explain the minimization techniques and universal gates.(K2)
3	Construct the logic circuits of various combinational circuits.(K3)
4	Explain the behavior of various sequential circuits.(K2,K4)

Unit No	Out Come/Bloom's Level		Topics/Activity	Reference Text book	Contact Periods	Delivery Method
1	CO1: Describe the different types of number systems and Boolean algebra.(K1)		**BASICS OF DIGITAL SYSTEMS**			Chalk & Talk, PPT & Tutorial.
		1.1	Review of number systems	T1,T2,R1	1	
		1.2	Binary arithmetic	T1,T2,R1	1	
		1.3	Unsigned and Signed Binary numbers	T1,T2,R1	1	
		1.4	1's and 2's complement of binary numbers	T1,T2,R1	1	
		1.5	9's and 10's complements of decimal numbers		1	
		1.6	Gray codes and Excess-3 codes	T1,T2,R1	1	
		1.7	Binary to Gray and Gray to Binary code conversion	T1,T2,R1	1	
		1.8	BCD addition and Excess-3 addition	T1,T2,R1	1	
		1.9	Review of Logic gates	T1,T2,R1	1	
		1.10	Properties of EX-OR gate	T1,T2,R1	1	
		1.11	CLASS TEST		1	
			TOTAL		11	
			SIMPLIFICATION OF BOOLEAN FUNCTIONS			
		2.1	Minimization Techniques: Boolean postulates and laws	T1,R1,R2	1	
		2.2	De-Morgan's theorems, Principle of Duality	T1,R1,R2	1	
		2.3	Boolean laws	T1,R1,R2	1	

2	CO2: Explain the minimization techniques and universal gates.(K2)	2.4	Canonical and standard forms of Boolean expressions	T1,R1,R2	1	Chalk & Talk, PPT & Tutorial
		2.5	Min-terms, Max terms, Sum of Products (SOP) and Product of Sums (POS)	T1,R1,R2	1	
		2.6	Minimization of Boolean expressions by using Boolean laws and theorems	T1,R1,R2	1	
		2.7	Karnaugh map Minimization: 3 and 4 variables	T1,R1,R2	1	
		2.8	Implementation of different logic circuits using only NAND gates	T1,R1,R2	1	
		2.9	Implementation of different logic circuits using only NOR gates	T1,R1,R2	1	
		2.10	CLASS TEST		1	
			TOTAL		10	
3	CO3: Construct the logic circuits of various combinational circuits.(K3)		**ARITHMATIC LOGIC CIRCUITS**			Chalk & Talk, PPT & Tutorial
		3.1	Half adder and Half Subtractor	T1,R1,R2	1	
		3.2	Full adder and Full Subtractor	T1,R1,R2	1	
		3.3	4-bit Parallel adder	T1,R1,R2	1	
		3.4	4-bit Adder/Subtractor	T1,R1,R2	1	
		3.5	Carry look ahead adder	T1,R1,R2	1	
		3.6	BCD adder	T1,R1,R2	1	
		3.7	Excess-3 adder	T1,R1,R2	1	
		3.8	Magnitude Comparators: 1-bit and 2-bit	T1,R1,R2	1	
		3.9	Magnitude Comparator: 4-bit	T1,R1,R2	1	
		3.10	Code converters: Binary to BCD code and BCD to Binary code converter	T1,R1,R2	1	
		3.11	BCD code to Excess-3 and Excess-3 to BCD code converter	T1,R1,R2	1	
		3.12	Binary to Excess-3 code and Excess-3 to Binary code converter	T1,R1,R2	1	
		3.13	Binary to Gray code and Gray code to Binary code converter	T1,R1,R2	1	
		3.14	CLASS TEST		1	
			TOTAL		14	
			COMBINATIONAL LOGIC CIRCUITS			
		4.1	Encoders: Octal to Binary	T1,R1,R2	1	
		4.2	Encoders: Decimal to BCD	T1,R1,R2	1	
		4.3	Decoders:2-Line to 4-Line	T1,R1,R2	1	
		4.4	Decoders:3-Line to 8-Line	T1,R1,R2	1	

4	CO3: Construct the logic circuits of various combinational circuits.(K3)	4.5	Priority encoder	T1,R1,R2	1	Chalk & Talk, PPT & Tutorial
		4.6	Multiplexers	T1,R1,R2	1	
		4.7	De-multiplexers	T1,R1,R2	1	
		4.8	Realization of Boolean functions using decoders	T1,R1,R2	1	
		4.9	Realization of Boolean functions using multiplexers	T1,R1,R2	1	
		4.10	Memory devices: Random Access Memory, Read only Memory	T1,R1,R2	1	
		4.11	Programmable Logic Devices: Programmable Read only Memory	T1,R1,R2	1	
		4.12	Programmable Logic Array	T1,R1,R2	1	
		4.13	Programmable Array Logic	T1,R1,R2	1	
		4.14	CLASS TEST		1	
			TOTAL		14	
5	CO4: Explain the behavior of various sequential circuits.(K2,K4)		**SEQUENTIAL LOGIC CIRCUITS**			Chalk & Talk, PPT & Tutorial
		5.1	Latches: RS-Latch using NAND and NOR Gates	T1,T2,R1	1	
		5.2	Flip-Flops: RS-Flip-Flop and D-Flip-Flop	T1,T2,R1	1	
		5.3	JK - Flip-Flop and T-Flip-Flop	T1,T2,R1		
		5.4	Master-Slave JK-Flip-Flop	T1,T2,R1	1	
		5.5	Truth Tables and Excitation Tables	T1,T2,R1	1	
		5.6	Flip-Flop conversions: RS-Flip-Flop to D-Flip-Flop	T1,T2,R1	1	
		5.7	RS-Flip-Flop to JK-Flip-Flop and RS-Flip-Flop to T-Flip-Flop	T1,T2,R1	1	
		5.8	JK-Flip-Flop to T-Flip-Flop and JK-Flip-Flop to D-Flip-Flop	T1,T2,R1	1	
		5.9	D-Flip-Flop to T-Flip-Flop and T-Flip-Flop to D-Flip-Flop	T1,T2,R1	1	
		5.10	Synchronous counters	T1,T2,R1	1	
		5.11	Asynchronous counters	T1,T2,R1	1	
		5.12	Up-Down counter	T1,T2,R1	1	
		5.13	Ring counter and Johnson counter	T1,T2,R1	1	
		5.14	Differences between Synchronous & Asynchronous counters. Shift Registers: Basic concepts of SISO, SIPO, PISO & PIPO.	T1,T2,R1	1	
		5.15	CLASS TEST		1	

				TOTAL	15	
	Content beyond Syllabus	1	Mealy and Moore machines	T1,R1,R2	1	
			TOTAL NO. OF PROPOSED CLASSES		65	

Text Books:

S.No.	AUTHORS/BOOK TITLE/EDITION(latest)/PUBLISHER/YEAR OF PUBLICATION
1	Morris Mano, "Digital Design", 4th Edition, Prentice Hall of India Pvt. Ltd., 2008 / Pearson Education (Singapore) Pvt. Ltd., New Delhi, 2003.
2	Charles H. Roth. "Fundamentals of Logic Design", 6th Edition, Thomson Learning, 2013.

Reference Books:

S.No.	AUTHORS/BOOK TITLE/EDITION(latest)/PUBLISHER/YEAR OF PUBLICATION
1	A. Anand Kumar, Fundamentals of Digital Circuits, 4th Ed., Prentice Hall India Pvt., Limited, 2016.
2	Rishabh Anand, Digital Electronics, 2nd Ed., KHANNA PUBLISHING HOUSE, 2014.
3	John F.Wakerly, "Digital Design", 4th Ed., Pearson/PHI, 2008.
4	Donald P. Leach and Albert Paul Malvino, "Digital Principles and Applications", 6th Edition, TMH, 2006.

Web Details

1	www.nptel.ac.in
2	www.slideshare.net
3	https://youtu.be/M0mx8S05v60

		Name	Signature with date
i.	Faculty-I	Mrs. G. B. Christina	
ii.	Faculty-II (for common Course)	Mr. V.Satya Kishore	
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vi.	Programme Coordinator	Dr. B. S. Rao	

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